R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 5 lines 12-20, page 20 line 19-page 21 line 4, and FIGS. 1-3 , as originally filed. Thus, no new matter has been added.

Although Applicant's representative does not necessarily agree with the Examiner's interpretation of the claimed master interface and the claimed slave interface, the claims have been amended to advance the prosecution. In particular, the claims have been amended to clarify that a master device and a slave device connectable to the claimed bus are not part of the claimed bus. Furthermore, the amendments clarify that the claimed first clock edge, the claimed second clock edge and the claimed registering steps are with respect to a system clock. As such, no new issues are believed to be raised. Entry of the amendments is respectfully requested under MPEP §714.13,II since the issue of how broadly to interpret the claims has been removed for appeal. If the amendments are not entered, Applicants respectfully request a concise explanation per MPEP §714.13,III.

INTERVIEW SUMMARY

Applicant's representative, John Ignatowski, spoke with Examiner Cleary on April 20 and 21, 2005 via telephone. Applicants representative requested clarification of the rejections which asserted that signals totally outside a system bus 20 of the Ohuchi were allegedly similar to claimed signals presented by the claimed bus. The Examiner stated that the slave processor 12 of Ohuchi was being treated as part of the system bus 20 of Ohuchi. No samples were presented. No agreement was reached regarding the claims.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 13 and 20 under 35 U.S.C. §102(b) as being anticipated by Ohuchi '847 has been obviated by appropriate amendment and should be withdrawn.

Ohuchi concerns a data processor with wait control allowing high speed access (Title).

Claim 1 provides a bus comprising a slave interface connectable to a slave device external to the bus and configured to (i) present a command signal to the slave device a delay after a first clock edge. In contrast, a signal WRRQIO (asserted similar to the claimed command signal) does not appear to be presented at a slave interface of a system bus 20 (asserted similar to the claimed bus) to a slave device external to the system bus 20. In particular, Ohuchi states that the signal WRRQIO is an internal

signal within a slave processor 12 (see column 3, lines 47-50 of Ohuchi) and the slave processor 12 of Ohuchi appears to be a slave device external to the system bus 20. As such, Ohuchi does not disclose or suggest a bus comprising a slave interface connectable to a slave device external to the bus and configured to (i) present a command signal to the slave device a delay after a first clock edge as presently claimed.

Claim 1 further provides a bus comprising a slave interface configured to receive a slave wait signal from the slave device. In contrast, a signal WAITI of Ohuchi (asserted similar to the claimed slave wait signal) does not appear to be received at a slave interface of the system bus 20 of Ohuchi from a slave device. In particular, Ohuchi shows that the signal WAITI is an internal signal within the slave processor 12 (see FIG. 4 of Ohuchi) and the slave processor 12 appears to be a slave device external to the system bus 20 of Ohuchi. As such, Ohuchi does not disclose or suggest a bus comprising a slave interface configured to receive a slave wait signal from a slave device external to the bus as presently claimed.

Claim 1 further provides a bus comprising a control logic configured to register the early command signal to generate the command signal. In contrast, Ohuchi does not appear to discuss a circuit of the system bus 20. The sections of Ohuchi cited in the Office Action appear to discuss circuitry within the slave

processor 12, which appears to be a slave device external to the system bus 20. Therefore, Ohuchi does not disclose or suggest a bus comprising a control logic configured to register an early command signal to generate a command signal as presently claimed.

Furthermore, the Office Action appears to be improperly relying on the teachings of the Applicant in forming the rejection of the claimed control logic. The Interview Summary from the Examiner states:

> If the bus is interpreted to include active devices, **such as the control logic 102 in Figure 1** [of the application], then the interfaces, and their included active devices, must also be considered as part to the bus. (Emphasis added)

As such, the Examiner is respectfully requested to either (i) provide evidence **from the prior art** that slave processors are considered by one of ordinary skill in the art to be part of a bus or (ii) withdraw the rejection.

Claim 1 further provides the control logic is configured to convert the slave wait signal into a bus wait signal (presented at the master interface of the bus to the master device). In contrast, Ohuchi appears to be silent regarding (i) a circuit of the system bus 20 converting the signal WAITI into the signal WAIT (asserted similar to the claimed bus wait signal) and (ii) presenting the signal WAIT at a master interface of the system bus 20. Therefore, Ohuchi does not disclose or suggest a control logic configured to convert a slave wait signal into a bus wait signal as presently claimed. Claims 13 and 20 provide language similar to

claim 1. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 2, 8, 9 and 14 under 35 U.S.C. §103(a) as being unpatentable over Ohuchi in view of Amagasaki '080 has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 3 and 15 under 35 U.S.C. §103(a) as being unpatentable over Ohuchi and Amagasaki in further view of Honma '662 has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 4 and 16 under 35 U.S.C. §103(a) as being unpatentable over Ohuchi in view of McIntyre '261 has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 5, 6, 17 and 18 under 35 U.S.C. §103(a) as being unpatentable over Ohuchi in further view of U.S. Patent Application Publication No. 2001/0010063 to Hirose et al. (hereafter Hirose) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 7 and 19 under 35 U.S.C. §103(a) as being unpatentable over Ohuchi and Hirose in further view of Pincus '583 has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 10, 11 and 12 under 35 U.S.C. §103(a) as being unpatentable over Ohuchi and Amagasaki in further view of Picazo '907 has been obviated by appropriate amendment and should be withdrawn.

Ohuchi concerns a data processor with wait control allowing high speed access (Title). Amagasaki concerns an integrated circuit device having tristate input buffer for reducing internal power use (Title). Hirose concerns a bus controller system for integrated circuit device with improved bus access efficiency (Title). Honma concerns a memory testing device for preventing excessive write and erasure (Title). McIntyre concerns a method and apparatus for burst protocol in a data processing system (Title). Picazo concerns a network hub with integrated bridge (Title). Pincus concerns a method and apparatus for memory access in a matrix processor computer (Title).

Claim 2 provides the master interface is configured to receive an early address signal from the master device before the first clock edge. In contrast, Ohuchi does not appear to show any relationship between a signal ADDRESS (asserted similar to the claimed early address signal) and the signal CLK (asserted to define the claimed first clock edge). Therefore, Ohuchi and Amagasaki, alone or in combination, does not appear to teach or suggest a master interface configured to receive an early address

signal from a master device before a first clock edge as presently claimed.

Claim 2 further provides the control logic is configured to (i) register the early address signal with the system clock to generate an address signal and (ii) decode the address signal to generate a device select signal. In contrast, Ohuchi appears to be silent regarding an AREG register in FIG. 5 (asserted to perform the claimed registering) using a system clock. Therefore, Ohuchi and Amagasaki, alone or in combination, do not appear to teach or suggest a control logic configured to register an early address signal with a system clock to generate an address signal and decode the address signal to generate a device select signal as presently claimed.

Claim 2 further provides the slave interface is configured to present the address signal and the device select signal to the slave device the delay after the first clock edge. In contrast, Ohuchi does not appear to show a signal AREG (asserted similar to the claimed address signal) being presented at a slave interface of the system bus 20. Therefore, Ohuchi and Amagasaki, alone or in combination, do not appear to teach or suggest a slave interface configured to present an address signal and a device select signal to a slave device a delay after a first clock edge as presently claimed. Claim 14 provides language similar to claim 2.

As such, claims 2 and 14 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 9 provides that the control logic comprises a plurality of registers configured to register a plurality of early signals with the system clock, each of the early signals being valid before the first clock edge to generate a plurality of signals the delay after the first clock edge. In contrast, Ohuchi appear to be silent regarding both (i) registering using a system clock and (ii) validity of the signals before the first clock edge of a system clock. Therefore, Ohuchi and Amagasaki, alone or in combination, do not teach or suggest a control logic comprising a plurality of registers configured to register a plurality of early signals with the system clock, each of the early signals being valid before a first clock edge to generate a plurality of signals a delay after the first clock edge as presently claimed. As such, claim 9 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 3 provides the master interface is configured to receive a no-address signal from the master device before the first clock edge. In contrast, one of ordinary skill in the art would not appear to understand a pass/fail decision signal S1 of Honma to be similar to the claimed no-address signal as asserted in the Office Action. The decision signal S1 of Honma appears to indicate if a device under test passes or fails a test (see Honma column 4,

lines 9-12). The claimed no-address signal may be asserted by a master device to prevent address signal decoding during a direct memory access transaction (see specification pave 11, lines 11-13). As such, the Examiner is respectfully requested to either (i) provide evidence why one of ordinary skill in the art would allegedly understand the decision signal S1 of Honma to be similar to the claimed no-address signal or (ii) withdraw the rejection.

Furthermore, Honma appears to be silent regarding the decision signal S1 of Honma (asserted similar to the claimed no-address signal) being received from a master device before a first clock edge of a system clock. In particular, the signal S1 of Honma appears to be generated and used internally to a test channel CH1, instead of being transferred from a master device to a bus. Therefore, Ohuchi, Amagasaki and Honma, alone or in combination, do not appear to teach or suggest a master interface configured to receive a no-address signal from a master device before a first clock edge as presently claimed. Claim 15 provides language similar to claim 3. As such, claims 3 and 15 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 4 provides the master interface is configured to receive an early burst request signal from the master device before the first clock edge (of a system clock). In contrast, McIntyre appears to be silent regarding a signal IBEQ (asserted similar to the claimed early burst request signal) being received before a

first clock edge of a system clock. Therefore Ohuchi and McIntyre, alone or in combination, do not appear to teach or suggest a master interface configured to receive an early burst request signal from a master device before a first clock edge of a system clock as presently claimed.

Claim 4 further provides the control logic is further configured to register the early burst request signal with the system clock to generate a burst request signal. In contrast, both Ohuchi and McIntyre appear to be silent regarding the signal IBEQ (asserted similar to the claimed early burst request signal) being registered with a system clock. Therefore, Ohuchi and McIntyre, alone or in combination, do not appear to teach or suggest a control logic configured to register an early burst request signal with a system clock to generate a burst request signal as presently claimed.

Claim 4 further provides the slave interface is configured to present the burst request signal to the slave device a delay after the first clock edge (of the system clock). In contrast, both Ohuchi and McIntyre appear to be silent regarding a presentation of a signal BREQ (asserted similar to the claimed burst request signal) a delay after a first clock edge of a system clock. Therefore, Ohuchi and McIntyre, alone or in combination, do not appear to teach or suggest a slave interface is further configured to present a burst request signal to a slave device a

delay after a first clock edge of a system clock as presently claimed. Claim 16 provides language similar to claim 4. As such, claims 4 and 16 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 5 provides the control logic (of the bus) is configured to arbitrate in response to a bus request signal and generate a bus grant signal. In contrast, Hirose appears to contemplate a structure different from as claimed. In particular, paragraph 0067 of Hirose indicates that the signal REQUEST is arbitrated by a chip A (a CPU) for control of a command bus 10. Hirose appears to be silent regarding the arbitration function being performed by the bus. Furthermore, the Office Action provides no evidence of motivation why one of ordinary skill in the art would move the arbitration function of Hirose from a command bus master (CPU chip A) into the command bus itself. Therefore, Ohuchi and Hirose, alone or in combination, do not appear to teach or suggest a control logic of a bus configured to arbitrate in response to a bus request signal and generate a bus grant signal as presently claimed. Claim 17 provides language similar to claim 5. As such, claims 5 and 17 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 10 provides that the control logic (of the bus) comprises an arbitration logic configured to generate a bus grant signal. In contrast, Picazo appears to teach a different structure

from as claimed. In particular, column 27, lines 43-45 of Picazo appear to indicate that the circuitry in FIG. 6A of Picazo, including the arbitration block 610, are part of an integrated hub/bridge. Therefore, the proposed combination of Ohuchi, Amagasaki and Picazo do not appear to teach or suggest the arbitration function within a bus as presently claimed. As such, the Examiner is respectfully requested to either (i) provide evidence why one of ordinary skill in the art would be motivated to move the arbitration function from the integrated hub/bridge of Picazo to a bus or (ii) withdraw the rejection.

Dependent claims 6, 7, 11, 12, 18 and 19 depended from independent claims 1 and 13, which are now believed to be allowable. Since the dependent claims contain all of the limitations of the independent claims, claims 6, 7, 11, 12, 18 and 19 are fully patentable over the cited references and the rejection should be withdrawn.

The Office Action fails to establish that Honma and Pincus are analogous art. Per *In re Oetiker*, the prior art reference must either be (i) in the field of Applicant's endeavor, or if not, (ii) then be reasonably pertinent to the particular problem with which the Applicant was concerned. In contrast, the Office Action provides no evidence that Honma and Pincus are (i) within the Applicant's field of endeavor or (ii) reasonably pertinent to a particular problem with which the Applicant was

concerned. Furthermore, the argument on page 14 of the Office Action how "one of ordinary skill in the art would naturally look to various methods of communication" appears to be a motivation argument, not an analogous art argument addressing the criteria of *In re Oetiker*. Therefore, *prima facie* obviousness has not been established. As such, the Examiner is respectfully requested to either (i) provide evidence how Honma and Pincus are within the Applicant's field of endeavor, or (ii) clearly identify the particular problem with which the Applicant was concerned and how Honma and Pincus pertain or (iii) withdraw the rejections of claims 3, 7, 15 and 19.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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